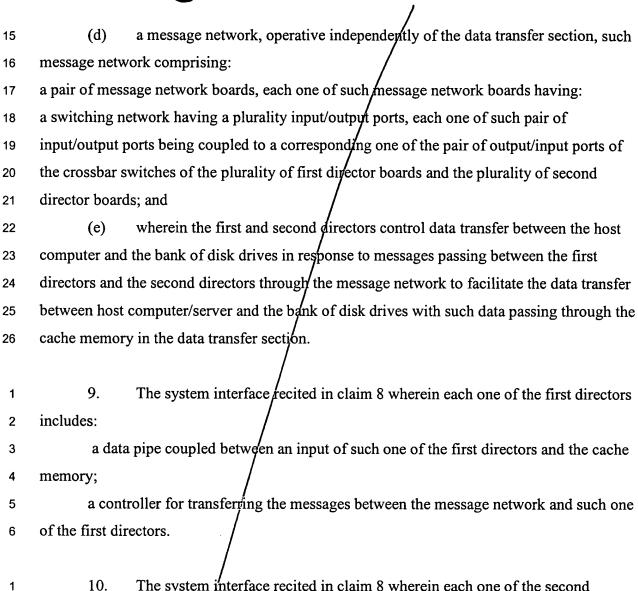


5	a controller for transferring the messages/between the message network and such o	ne
6	of the first directors.	
1	3. The system interface recited in claim 1 wherein each one of the second	
2	directors includes:	
3	a data pipe coupled between an input of such one of the second directors and the	
4	cache memory;	
5	a controller for transferring the messages between the message network and such o	ne
6	of the second directors.	
1	4. The system interface recited in claim 2 wherein each one of the second	
2	directors includes:	
3	a data pipe coupled between an input of such one of the second directors and the	
4	cache memory;	
5	a controller for transferring the messages between the message network and such o	ne
6	of the second directors.	
1	5. The system interface recited in claim 1 wherein each one of the first directo	rs
2	includes:	
3	a data pipe coupled between an input of such one of the first directors and the cach	ıe
4	memory;	
5	a microprocessor, and	
6	a controller coupled to the microprocessor and the data pipe for controlling the	
7	transfer of the messages between the message network and such one of the first directors a	nd
8	for controlling the data between the input of such one of the first directors and the cache	
9	memory.	
1	6. The system interface recited in claim 1 wherein each one of the second	
2	directors includes	
3	a data pipe coupled between an input of such one of the second directors and the	
4	cache memory;	



5	a microprocessor; and
6	a controller coupled to the microprocessor and the data pipe for controlling the
7	transfer of the messages between the message network and such one of the second directors
8	and for controlling the data between the input of such one of the second directors and the
9	cache memory.
1	7. The system interface recited in claim 5 wherein each one of the second
2	directors includes:
3	a data pipe coupled between an input of such one of the second directors and the
4	cache memory;
5	a microprocessor; and
6	a controller coupled to the microprocessor and the data pipe for controlling the
7	transfer of the messages between the message network and such one of the second directors
8	and for controlling the data between the input of such one of the second directors and the
9	cache memory.
1	8. A data storage system for transferring data between a host computer/server
2	and a bank of disk drives through a system interface, such system interface comprising:
3	(a) a plurality of first director boards coupled to host computer/server, each one
4	of the first director boards having
5	(i) a plurality of first directors; and
6	(ii) a crossbar switch having input/output ports coupled to the first
7	directors on such one of the first director boards and a pair of output/input ports;
8	(b) a plurality of second director boards coupled to the bank of disk drives, each
9	one of the second director boards having:
10	(i) a plurality of second directors; and
11	(ii) a crossbar switch having input/output ports coupled to the second
12	directors on such one of the second director boards and a pair of output/input ports;
13	(c) a data transfer section having a cache memory, such cache memory being
14	coupled to the plurality of first and second directors;





10. The system interface recited in claim 8 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;

a controller for transferring the messages between the message network and such one of the second directors.

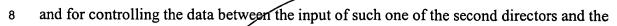
11. The system interface recited in claim 9 wherein each one of the second directors includes:

a data pipe coupled between an input of such one of the second directors and the cache memory;



5	a controller for transferring the messages between the message network and such one
6	of the second directors.
1	12. The system interface recited in claim 8 wherein each one of the first directors
2	includes:
3	a data pipe coupled between an input of such one of the first directors and the cache
4	memory;
5	a microprocessor; and
6	a controller coupled to the microprocessor and the data pipe for controlling the
7	transfer of the messages between the message network and such one of the first directors and
8	for controlling the data between the input of such one of the first directors and the cache
9	memory.
1	13. The system interface recited in claim 8 wherein each one of the second
2	directors includes:
3	a data pipe coupled between an input of such one of the second directors and the
4	cache memory;
5	a microprocessor; and
6	a controller coupled to the microprocessor and the data pipe for controlling the transfer of the
7	messages between the message network and such one of the second directors and for
8	controlling the data between the input of such one of the second directors and the cache
9	memory.
1	14. The system interface recited in claim 12 wherein each one of the second
2	directors includes:
3	a data pipe coupled between an input of such one of the second directors and the
4	cache memory;
5	a microprocessor; and
6	a controller coupled to the microprocessor and the data pipe for controlling the
7	transfer of the messages between the message network and such one of the second directors





9 cache memory.